



UTD405

Power MOSFET

P-CHANNEL ENHANCEMENT MODE

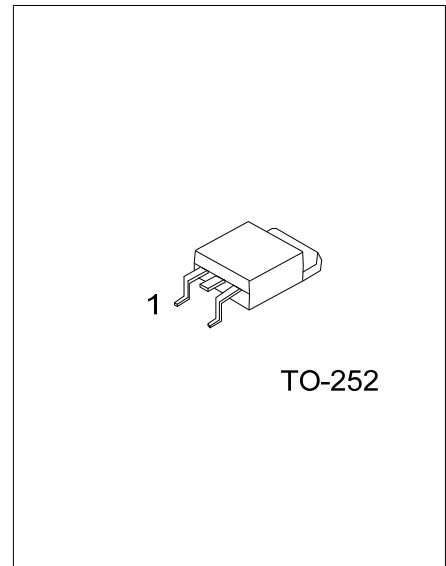
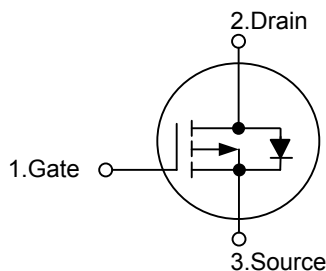
DESCRIPTION

The **UTD405** can provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance by using advanced trench technology. This device is well suited for high current load applications with the excellent thermal resistance.

FEATURES

- * $R_{DS(ON)} = 32m\Omega @ V_{GS} = -10V$
- * Low capacitance
- * Low gate charge
- * Fast switching capability
- * Avalanche energy specified

SYMBOL



*Pb-free plating product number: UTD405L

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
UTD405-TN3-R	UTD405L-TN3-R	TO-252	G	D	S	Tape Reel
UTD405-TN3-T	UTD405L-TN3-T	TO-252	G	D	S	Tube

UTD405L-TN3-R (1)Packing Type (2)Package Type (3)Lead Plating		(1) R: Tape Reel, T: Tube (2) TN3: TO-252 (3) L: Lead Free Plating, Blank: Pb/Sn
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■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-18	A
Pulsed Drain Current	I_{DM}	-40	A
Avalanche Current	I_{AR}	-18	A
Repetitive Avalanche Energy(L=0.1mH)	E_{AR}	40	mJ
Power Dissipation	P_D	2.5	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient	θ_{JA}		40	50	$^{\circ}\text{C/W}$

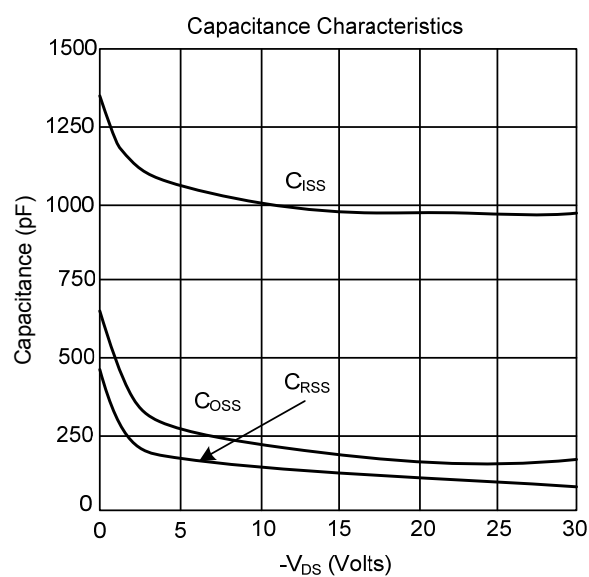
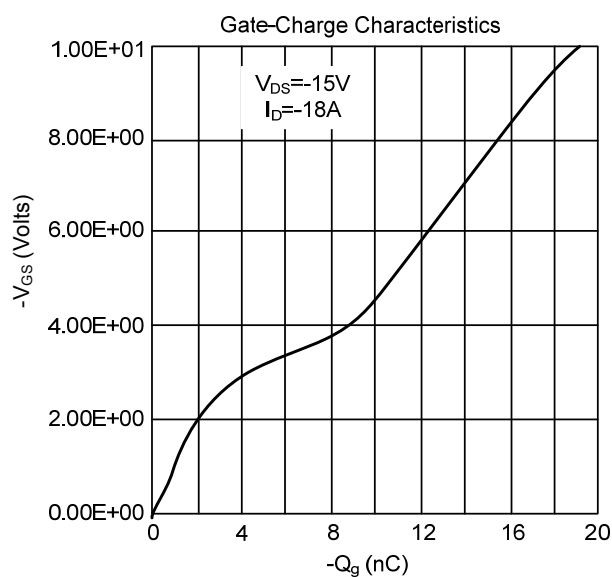
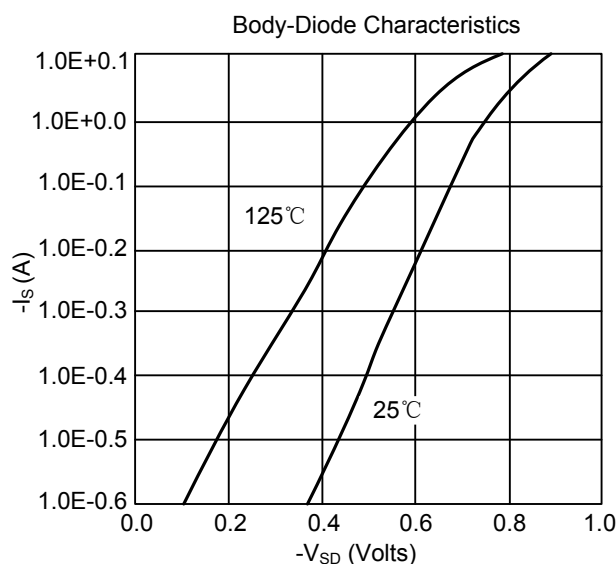
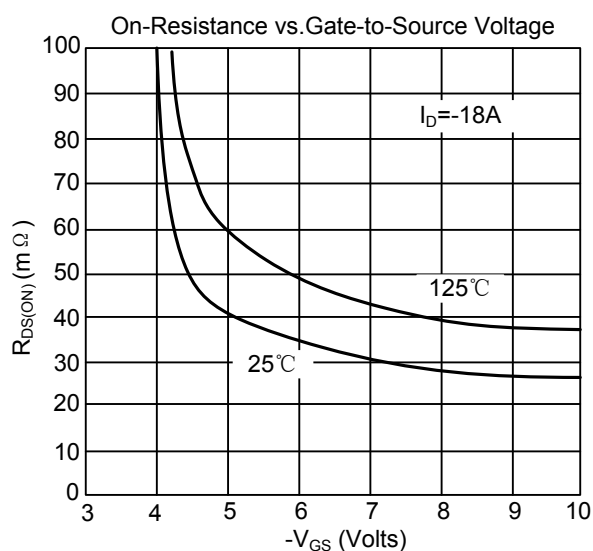
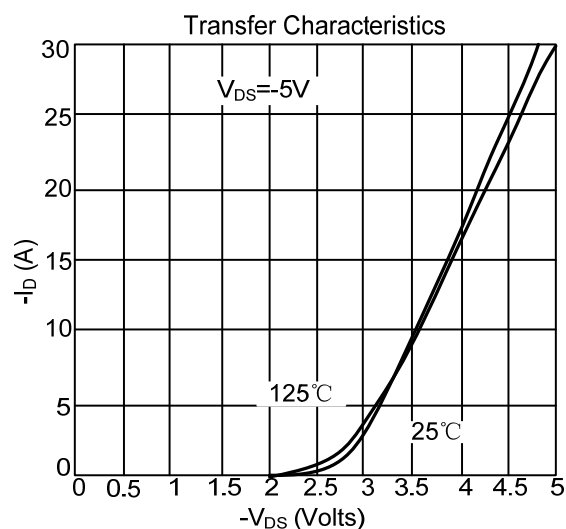
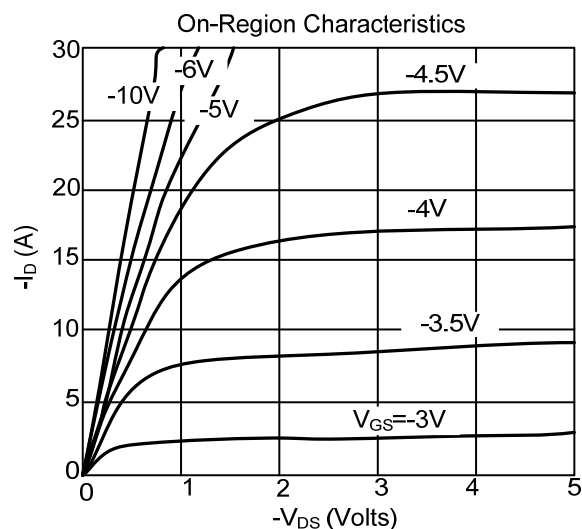
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0 V, I _D =-250 μA	-30			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-24 V, V _{GS} =0 V		-0.003	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =0 V, V _{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate-Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250 μA	-1.2	-2	-2.4	V
On state drain current	I _{D(ON)}	V _{GS} =-10V, V _{DS} =-5V	-40			A
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10 V, I _D =-18A		24.5	32	mΩ
		V _{GS} =-4.5 V, I _D =-10A		41	60	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =-15 V, V _{GS} =0V, f=1MHz		920	1100	pF
Output Capacitance	C _{OSS}			190		pF
Reverse Transfer Capacitance	C _{RSS}			122		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =-15V, V _{GS} =-10V, I _D =-18 A		18.7	23	nC
Gate-Source Charge	Q _{GS}			2.54		nC
Gate-Drain Charge	Q _{GD}			5.4		nC
Turn-ON Delay Time	t _{D(ON)}	V _{GS} =-10V,V _{DS} =-15V, R _L =0.82Ω, R _{GEN} =3Ω		9	13	ns
Turn-ON Rise Time	t _R			25	35	ns
Turn-OFF Delay Time	t _{D(OFF)}			20	30	ns
Turn-OFF Fall-Time	t _F			12	18	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V _{SD}	I _S =-1A,V _{GS} =0V		-0.76	-1	V
Maximum Continuous Drain-Source Diode Forward Current	I _S				-18	A
Body Diode Reverse Recovery Time	t _{RR}	I _F =-18A, dI/dt=100A/μs		21.4	26	ns
Body Diode Reverse Recovery Charge	Q _{RR}	I _F =-18A, dI/dt=100A/μs		13	16	nC

Notes: 1. Pulse width limited by $T_{J(MAX)}$

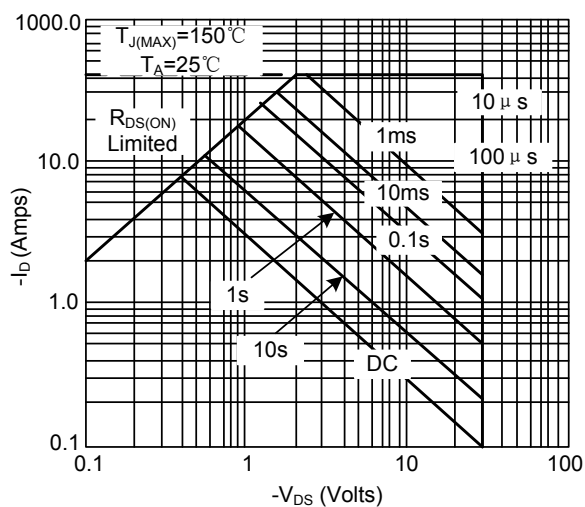
2. Pulse width $\leq 300\mu\text{s}$, duty cycle 0.5% max.

■ TYPICAL CHARACTERISTICS

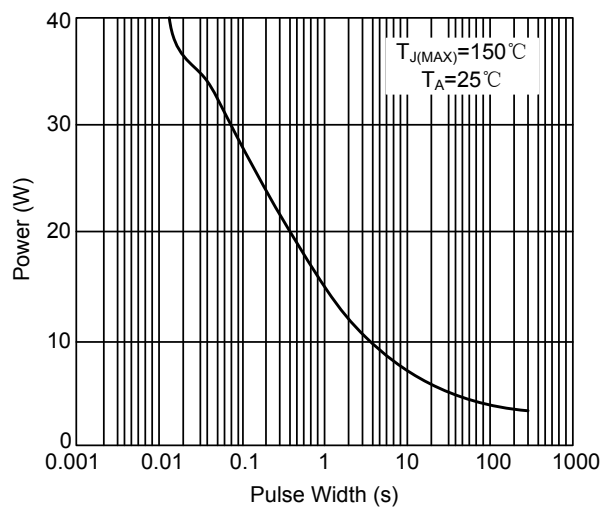


TYPICAL CHARACTERISTICS(Cont.)

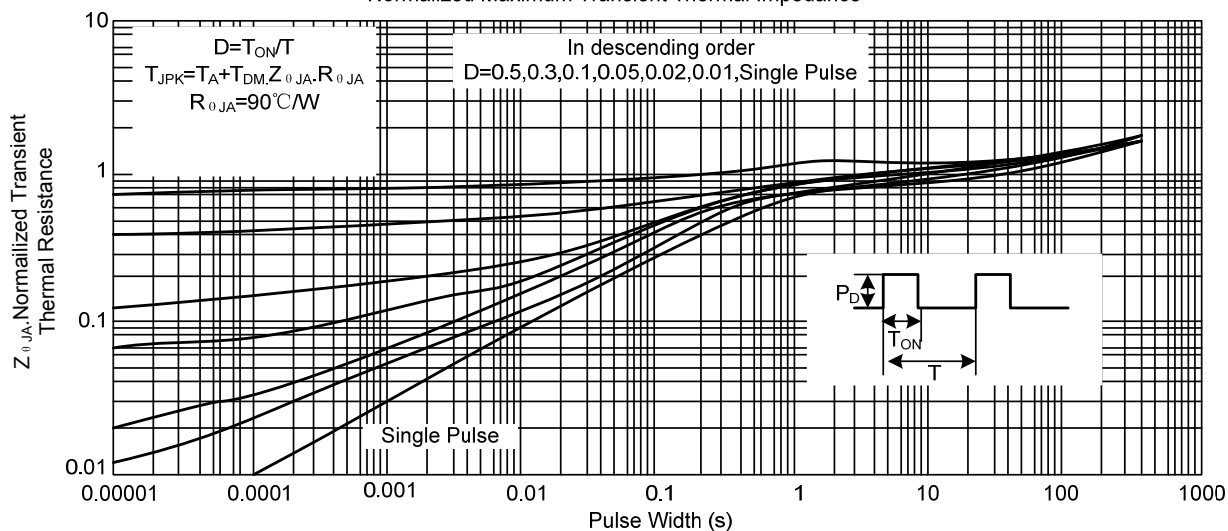
Maximum Forward Biased Safe Operating Area



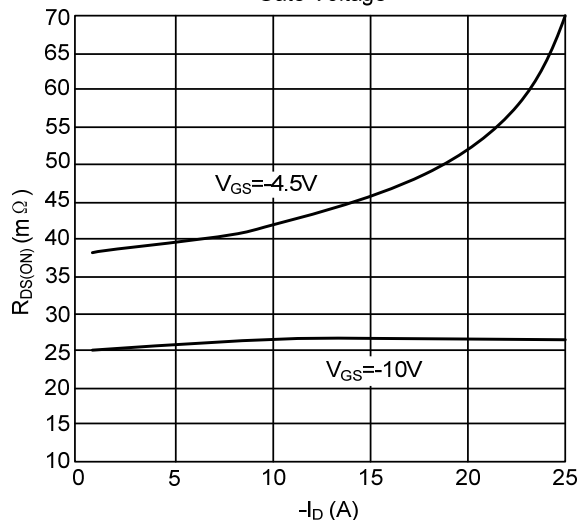
Single Pulse Power Rating Junction-to-Ambient



Normalized Maximum Transient Thermal Impedance



On-Resistance vs. Drain Current and Gate Voltage



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