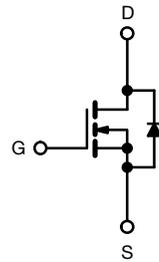
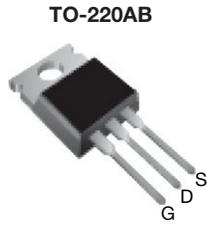


Power MOSFET



N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche, and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Low $R_{DS(on)}$
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


 Available
RoHS*
 Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching
- Hard switched and high frequency circuits

PRODUCT SUMMARY	
V_{DS} (V)	500
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.26
Q_g max. (nC)	120
Q_{gs} (nC)	34
Q_{gd} (nC)	54
Configuration	Single

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRFB18N50KPbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	500	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed drain current ^a	I_{DM}	68		
Linear derating factor		1.8	W/ $^\circ\text{C}$	
Single pulse avalanche energy ^b	E_{AS}	370	mJ	
Repetitive avalanche current ^a	I_{AR}	17	A	
Repetitive avalanche energy ^a	E_{AR}	22	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	220	W
Peak diode recovery dV/dt ^c		dV/dt	7.8	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) ^d	For 10 s	300		
Mounting torque	6-32 or M3 screw	10	N	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 2.5\text{ mH}$, $R_G = 25\text{ }^\circ\Omega$, $I_{AS} = 17\text{ A}$
- $I_{SD} \leq 17\text{ A}$, $dI/dt \leq 376\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient ^a	R _{thJA}	-	58	°C/W
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	
Maximum junction-to-case (drain) ^a	R _{thJC}	-	0.56	

Note

a. R_{th} is measured at T_J approximately 90 °C

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	500	-	-	V	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.59	-	V/°C	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3.0	-	5.0	V	
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V	-	-	± 100	nA	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V	-	-	50	μA	
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C	-	-	250		
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A ^b	-	0.26	0.29	Ω	
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 10 A	6.4	-	-	S	
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	2830	-	pF	
Output capacitance	C _{oss}		-	330	-		
Reverse transfer capacitance	C _{rss}		-	38	-		
Output capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	3310	-	
			V _{DS} = 400 V, f = 1.0 MHz	-	93	-	
Effective output capacitance	C _{oss eff.}	V _{DS} = 0 V to 400 V ^c	-	155	-		
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 17 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	120	nC
Gate-source charge	Q _{gs}			-	-	34	
Gate-drain charge	Q _{gd}			-	-	54	
Turn-on delay time	t _{d(on)}	V _{GS} = 10 V	V _{DD} = 250 V, I _D = 17 A, R _G = 7.5 Ω, see fig. 10 ^b	-	22	-	ns
Rise time	t _r			-	60	-	
Turn-off delay time	t _{d(off)}			-	45	-	
Fall time	t _f			-	30	-	
Gate input resistance	R _g	f = 1 MHz, open drain		0.7	-	2.7	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	17	A
Pulsed diode forward current ^a	I _{SM}			-	-	68	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 17 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 17 A, dI/dt = 100 A/μs ^b		-	520	780	ns
Body diode reverse recovery charge	Q _{rr}			-	5.3	8.0	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
- c. C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

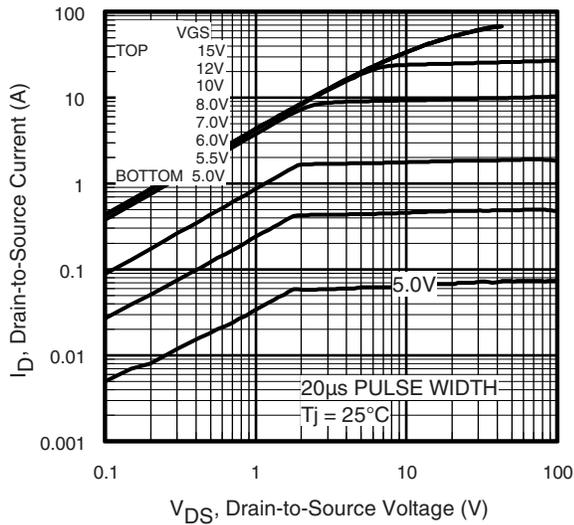


Fig. 1 - Typical Output Characteristics

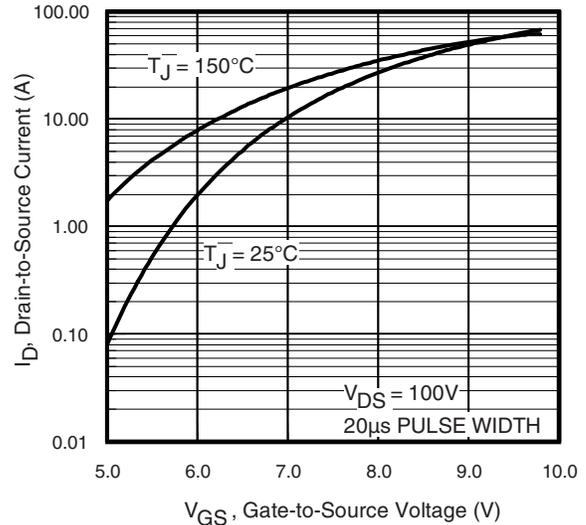


Fig. 3 - Typical Transfer Characteristics

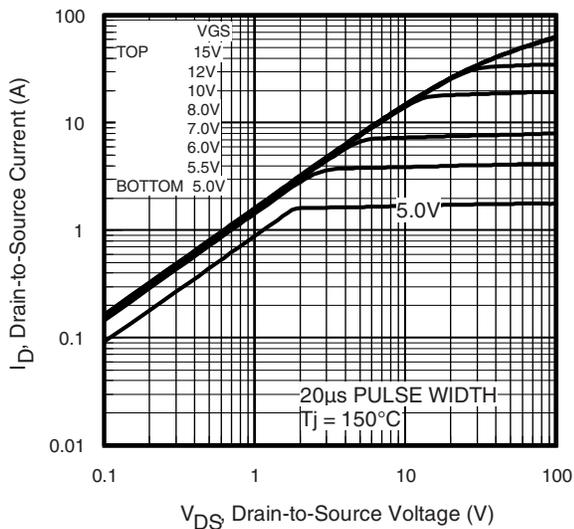


Fig. 2 - Typical Output Characteristics

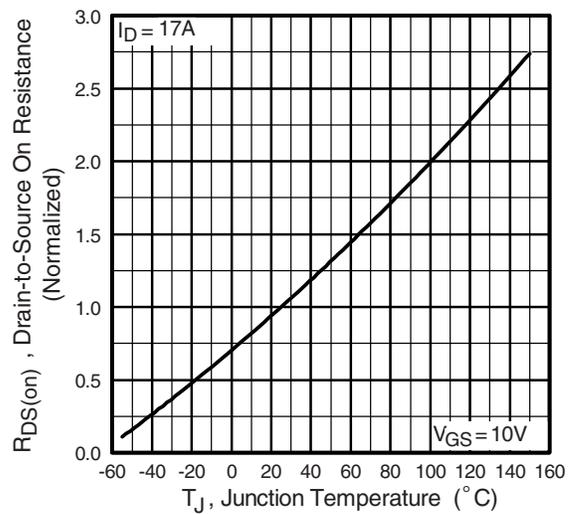


Fig. 4 - Normalized On-Resistance vs. Temperature

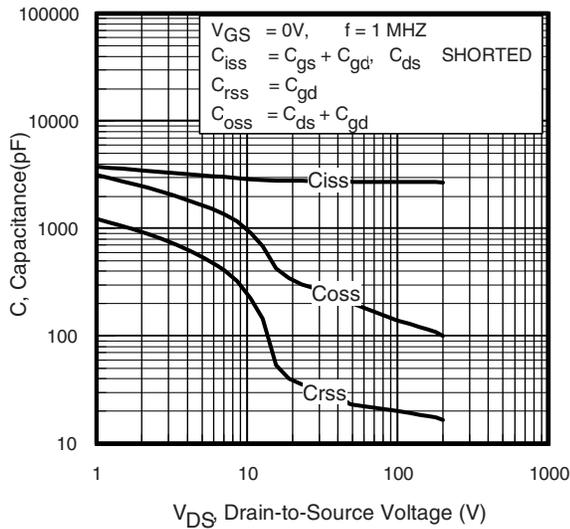


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

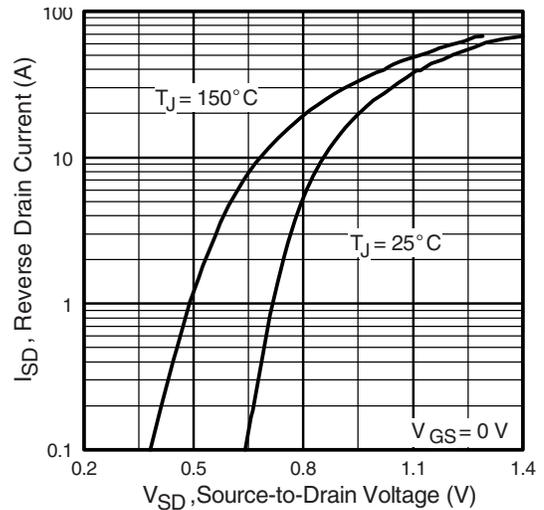


Fig. 7 - Typical Source-Drain Diode Forward Voltage

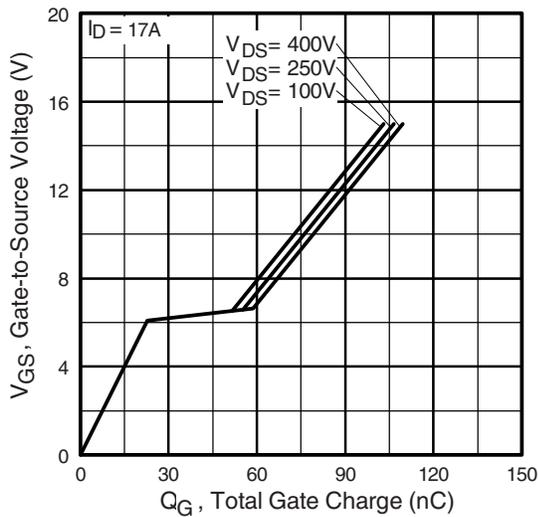


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

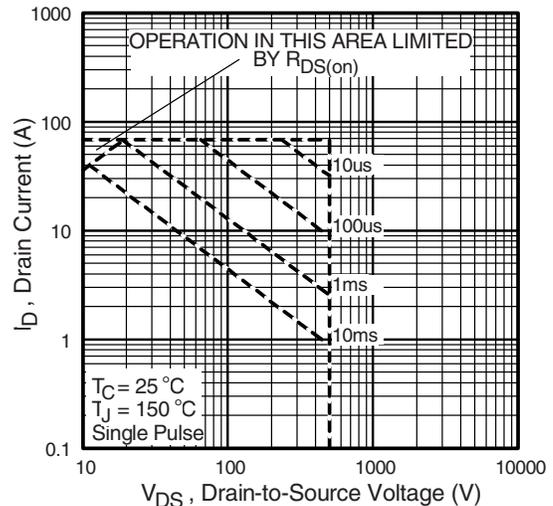


Fig. 8 - Maximum Safe Operating Area

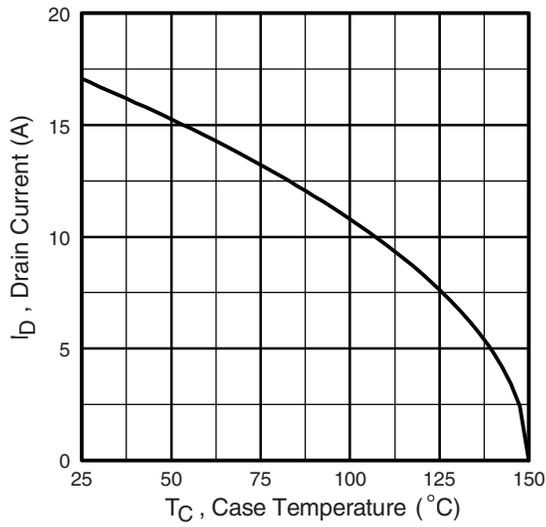


Fig. 9 - Maximum Drain Current vs. Case Temperature

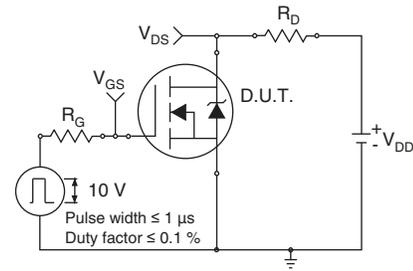


Fig. 10a - Switching Time Test Circuit

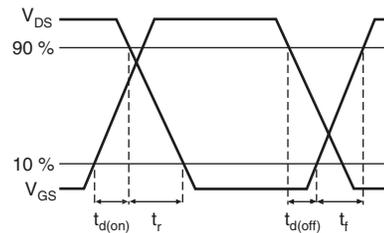


Fig. 10b - Switching Time Waveforms

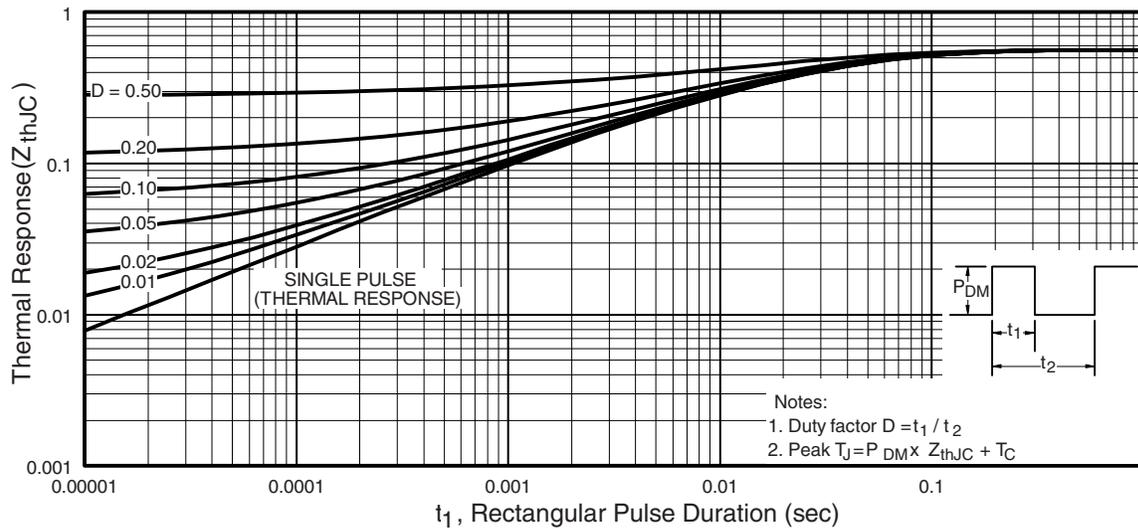


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

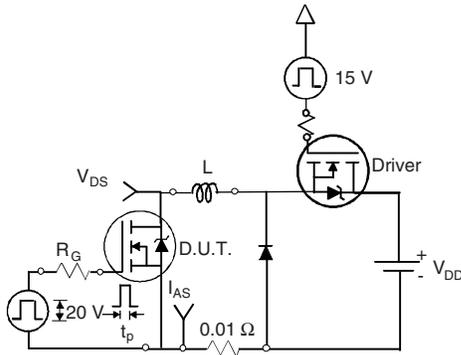


Fig. 12a - Unclamped Inductive Test Circuit

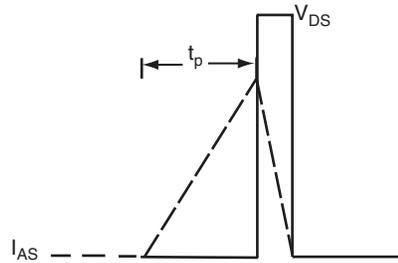


Fig. 12b - Unclamped Inductive Waveforms

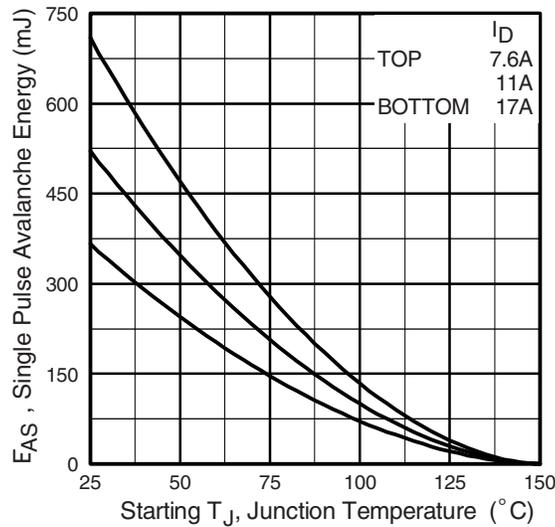


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

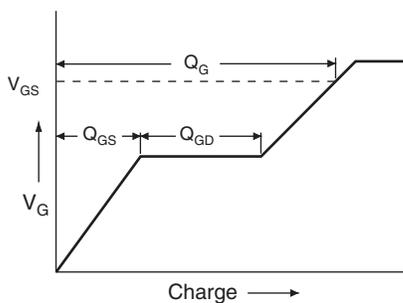


Fig. 13a - Basic Gate Charge Waveform

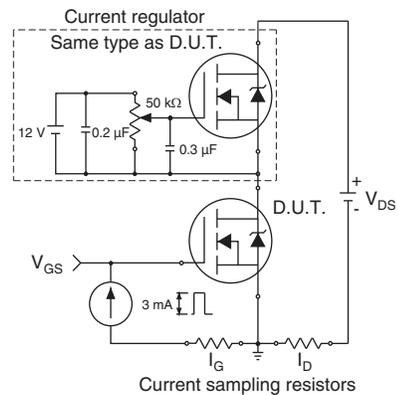
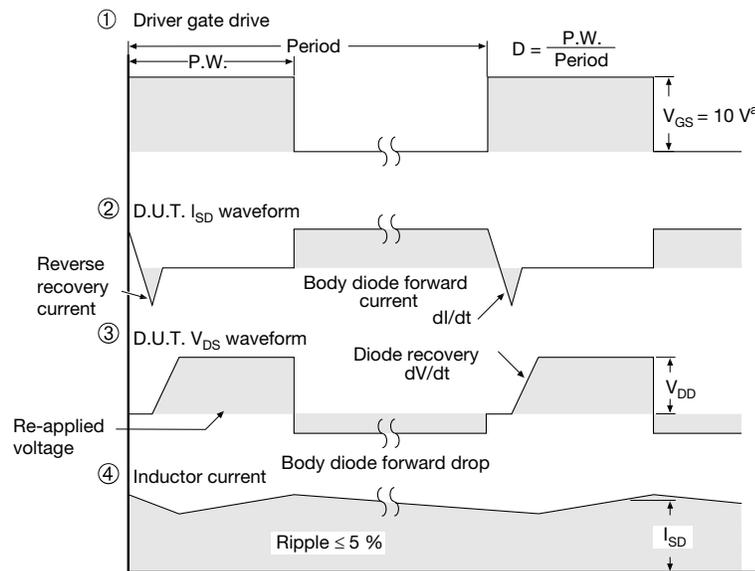
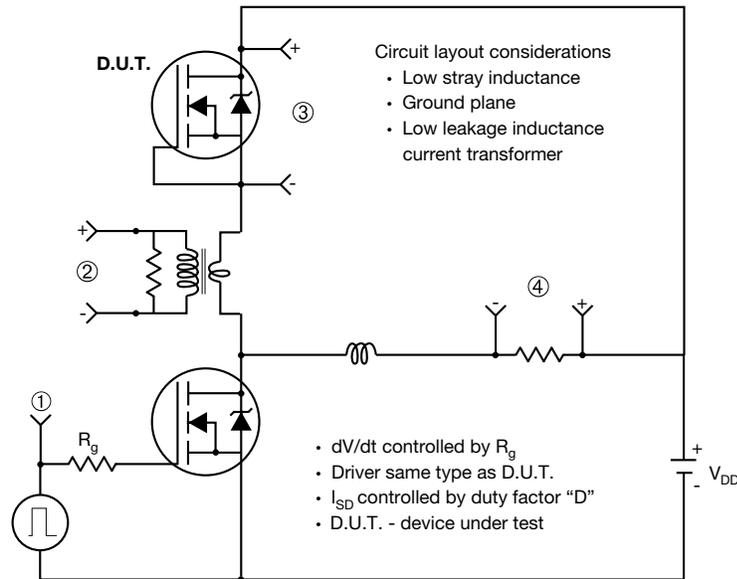


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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